Scholar **All articles** - **Recent articles** Results **1 - 10** of about **6,870** for **static timing (combinatorial**

All Results
K Keutzer
J Fishburn
S Devadas
M Orshansky
M Smith

Clock skew optimization - all 3 versions »
JP Fishburn - Computers, IEEE Transactions on, 1990 - ieeexplore.ieee.org
... variations [1], [2]. **Clock** skew can limit the clocking rate of a synchronous system or cause malfunction at any **clock** rate. Some **static timing** analyzers [3 ...
Cited by 217 - Related Articles - Web Search

Chip layout optimization using critical path weighting - all 3 versions »
AE Dunlop, VD Agrawal, DN Deutsch, MF Jukl, P ... - Annual ACM IEEE Design Automation Conference, 1984 - portal.acm.org
... analysis data produced by a **static timing** analysis program ... If the **clock** goes through gating logic, then ... assignment for latch-to-latch **combinational** data path ...
Cited by 120 - Related Articles - Web Search

Method and structure for use in **static timing** verification of synchronous circuits - all 2 versions »
AR Wang, R Rudell - US Patent 5,579,510; 1996 - Google Patents
... are represented in the **static timing** verification using ... a **clock** signal, or synchronous **timing** constraints ... the output signal of that **combinational** logic element ...
Cited by 13 - Related Articles - Web Search

Automated low-power technique exploiting multiple supply voltagesapplied to a media processor - all 5 versions »
K Usami, M Igarashi, F Minami, T Ishikawa, M ... - Solid-State Circuits, IEEE Journal of, 1998 - ieeexplore.ieee.org
... at flip-flops but also at **combinational** logic **gates**. ... setup and hold times using **static timing** analysis. For **clock**, we performed **timing** verification using SPICE ...
Cited by 135 - Related Articles - Web Search - BL Direct

[BOOK] Application-specific integrated circuits - all 6 versions »
MJS Smith - 1997 - www-ee.eng.hawaii.edu
... 55 2.3 CMOS Design Rules 58 2.4 **Combinational** Logic Cells ... 170 4.1.1 Metal-Metal Antifuse
172 4.2 **Static** RAM 174 ... ACT 3 Logic Modules 196 5.1.5 **Timing** Model and ...
Cited by 181 - Related Articles - Cached - Web Search - Library Search

Clock-delayed domino for adder and **combinational** logic design - all 4 versions »
G Yee, C Sechen - Computer Design: VLSI in Computers and Processors, 1996. ..., 1996 - ieeexplore.ieee.org
... **gates** by simply replacing the **static gate** library with a ... Once a **combinational** logic netlist has been generated ... A circuit **timing** analysis and CDLD insertion tool ...
Cited by 33 - Related Articles - Web Search

First-order incremental block-based statistical **timing** analysis - all 15 versions »
C Visweswariah, K Ravindran, K Kalafala, SG Walker ... - Proceedings of the 41st annual conference on Design ..., 2004 - portal.acm.org